
Errata

- The SPI can Send Wrong Byte
- Reset During EEPROM Write
- SPI Interrupt Flag can be Undefined After Reset
- Verifying EEPROM in System

4. The SPI can Send Wrong Byte

If the SPI is in master mode, it will restart the old transfer if new data is written on the same clock edge as the previous transfer is finished.

Problem Fix/Workaround

When writing to the SPI, first wait until it is ready, then write the byte to transmit.

3. Reset During EEPROM Write

If reset is activated during EEPROM write the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

2. SPI Interrupt Flag can be Undefined After Reset

In certain cases when there are transitions on the SCK pin during reset, or the SCK pin is left unconnected, the start-up value of the SPI interrupt flag is be unknown. If the flag is not reset before enabling the SPI interrupt, a pending SPI interrupt may be executed.

Problem Fix/Workaround

Clear the SPI interrupt flag before enabling the interrupt.

1. Verifying EEPROM in System

EEPROM verify in In-System Programming mode cannot operate with maximum clock frequency. This is independent of the SPI clock frequency.

Problem Fix/Workaround

Reduce the clock speed, or avoid using the EEPROM verify feature.



8-Bit AVR[®]
Microcontroller
with 4K bytes of
In-System
Programmable
Flash

AT90S4414
Rev. A & B
Errata Sheet

